File: 12969USF.RTF

# HIGH VOLTAGE LDMOS TRANSISTOR HAVING AN ISOLATED STRUCTURE

## BACKGROUND OF THE INVENTION

### Field of Invention

[0001] The present invention relates to semiconductor devices, and more particularly to a lateral power MOSFET.

### Description of Related Art

[0002] The development of single chip processes for integrating power switches with control circuitry is a major trend in the field of power IC development. The LDMOS (lateral double diffusion MOS) process in particular is currently being applied to manufacture monolithic ICs. The LDMOS process involves performing planar diffusion on the surface of a semiconductor substrate to form a main current path oriented in the lateral direction. Since the lateral MOSFET is manufactured using a typical IC process, the control circuit and the lateral power MOSFET can be integrated onto a monolithic power IC.

[0003] FIG. **1** shows a block diagram of a power converter. A transformer **200** is the load of a monolithic power IC **500**. A LDMOS transistor **100** having a drain electrode **10**, a source electrode **20** and a polysilicon gate electrode **40** is used to switch the transformer **200**. A resistor **400** is utilized to sense a switching current $I_S$ of the LDMOS transistor **100** for power control. A controller **300** generates a control signal to drive the LDMOS transistor **100** for power conversion. In order to reduce the cost and optimize switching performance, the controller **300** and the LDMOS transistor **100** are implemented on the

same substrate. The LDMOS process employing a reduced surface electric field (RESURF) technique using low thickness of EPI or N-well can achieve a high voltage with low on-resistance.

[0004] Recently, development of high-voltage LDMOS transistors have been proposed by Klas H. Eklund, in U.S. Patent **4,811,075** entitled "High Voltage MOS Transistors"; by Vladimir Rumennik and Robert W. Busse, in U.S. Patent **5,258,636** entitled "Narrow Radius Tips for High Voltage Semiconductor Devices with Interdigitated Source and Drain Electrodes"; However, the drawback of theses prior arts are that aforementioned LDMOS transistor have higher on-resistance. High voltage and low on-resistance LDMOS transistor, for example, are proposed by Klas H. Eklind, in U.S. Patent **5,313,082** entitled "High Voltage MOS Transistor with a Low On-Resistance"; by Gen Tada, Akio Kitamura, Masaru Saito, and Naoto Fujishima, in U.S. Patent **6,525,390 B2** entitled "MIS Semiconductor Device with Low On Resistance and High Breakdown Voltage"; by Vladimir Rumennik, Donald R. Disney, and Janardhanan S. Ajit, in U.S. Patent **6,570,219 B1** entitled "High-voltage Transistor with Multi-layer Conductor Region"; by Masaaki Noda, in U.S. Patent **6,617,652 B2** entitled "High Breakdown Voltage Semiconductor Device". Although a high voltage and low on-resistance LDMOS transistor can be manufactured, the complexity of the production processes increases the production cost and/or reduces the production yield. Another disadvantage of these proposed transistors is none-isolated source structure. A none-isolated transistor current could flow around the substrate. This may generate noise interference in the control circuit **300**. Besides, the switching current $\mathbf{I_S}$ of the LDMOS transistor **100** can generate a ground bounce to disturb the control circuit **300**. Furthermore, only an isolated LDMOS transistor can restrict the current flow. Therefore

the switching current $I_S$ through the resistor **400** can be accurately measured. In order to solve these problems, the present invention proposes a LDMOS structure to achieve a high breakdown voltage, low on-resistance and isolated transistor for the monolithic integration.

## SUMMARY OF THE INVENTION

[0005] An isolated high voltage LDMOS transistor according to the present invention includes a P-substrate. The LDMOS transistor also includes a first diffusion region and a second diffusion region having N conductivity-type ions to form an N-well in the P-substrate. The first diffusion region further comprises an extended drain region. A drain diffusion region having N+ conductivity-type ions forms a drain region. The drain region is formed in the extended drain region. A third diffusion region containing P conductivity-type ions forms a P-field and a plurality of divided P-fields located in the extended drain region. The divided P-fields are located nearer to the drain region than the P-field. A source diffusion region having N+ conductivity-type ions forms a source region. A contact diffusion region containing P+ conductivity-type ions forms a contact region. A fourth diffusion region containing P conductivity-type ions forms an isolated P-well for preventing from breakdown. The isolated P-well located in the second diffusion region encloses the source region and the contact region. The P-field and the divided P-fields located in the extended drain region of the N-well form junction-fields in the N-well to deplete a drift region. A channel is thus developed between the source region and the drain region extending through the N-well. The divided P-fields reduce the on-resistance of the channel. A polysilicon gate electrode is disposed above the channel to control a current flow in the channel. Furthermore, the portion of the N-well generated

by the second diffusion region provides a low-impedance path for the source region to restrict the current flow in between the drain region and the source region.

[0006] It is to be understood that both the foregoing general descriptions and the following detailed descriptions are exemplary, and are intended to provide further explanation of the invention as claimed. Still further objects and advantages will become apparent from a consideration of the ensuing description and drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0008] FIG. **1** shows a block schematic of a power converter.

[0009] FIG. **2** is a cross-sectional view of a LDMOS transistor according to a preferred embodiment of the present invention.

[0010] FIG. **3** shows a top view of the LDMOS transistor shown in FIG. **2**.

[0011] FIG. **4** shows the electrical field distribution when a 650V voltage is applied to a drain region of the LDMOS transistor according to a preferred embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] FIG. **2** is a cross-sectional view of an LDMOS transistor **100**. The LDMOS transistor **100** includes a P-substrate **90**. The LDMOS transistor **100** further includes a first diffusion region **33** and a second diffusion region **37** containing N conductivity-type

ions to form an N-well **30** in the P-substrate **90**. The first diffusion region **33** further comprises an extended drain region **50**. A drain diffusion region **53** having N+ conductivity-type ions in the N-well **30** formed by the first diffusion region **33**, develops a drain region **52** in the extended drain region **50**. A third diffusion region containing P conductivity-type ions forms a P-field **60**, divided P-fields **61** and **62** located in the extended drain region **50**. The divided P-fields **61** and **62** are nearer to the drain region **52** than the P-field **60**. A source diffusion region **55** having N+ conductivity-type ions in the N-well **30** formed by the second diffusion region **37**, develops a source region **56**. A contact diffusion region **57** containing P+ conductivity-type ions in the N-well **30** formed by the second diffusion region **37**, develops a contact region **58**. A fourth diffusion region **67** containing P conductivity-type ions in the N-well **30** formed by the second diffusion region **37**, develops an isolated P-well **65** for preventing from breakdown. The isolated P-well **65** encloses the source region **56** and the contact region **58**. The P-field **60**, the divided P-fields **61** and **62** form junction-fields in the N-well **30** to deplete a drift region.

[0013] A channel is developed between the source region **56** and the drain region **52** extending through the N-well **30**. The divided P-fields **61** and **62** are further capable of reducing the on-resistance of the channel. A thin gate oxide **81** and a thick field oxide **87** are formed over the P-substrate **90**. A polysilicon gate electrode **40** is disposed above the portion of the gate oxide **81** and the field oxide **87** to control a current flow in the channel. A drain-gap **71** is formed between the drain diffusion region **53** and the field oxide **87** to maintain a space between the drain diffusion region **53** and the field oxide **87**. A source-gap **72** is formed between the field oxide **87** and the isolated P-well **65** to maintain a space between the field oxide **87** and the isolated P-well **65**. Proper placement of the drain-gap **71** and the source-gap **72** can substantially increase the breakdown voltage of the

LDMOS transistor **100**. The drain-gap **71** can further reduce the on-resistance of the channel.

[0014] Insulation layers **85** and **86** cover the polysilicon gate **40**, the field oxide **87** and a field oxide **88**. The insulation layers **85** and **86** are, for example, made of silicon dioxide. A drain metal contact **15** is a metal electrode for contacting with the drain diffusion region **53**. A source metal contact **25** is a metal electrode for contacting with the source diffusion region **55** and the contact diffusion region **57**.

[0015] FIG. **3** is a top view of proposed LDMOS transistor **100** shown in FIG. **2**. The LDMOS transistor **100** includes a drain electrode **10**, a source electrode **20**, the polysilicon gate electrode **40**, a bonding pad **12** for the drain electrode **10**, a bonding pad **22** for the source electrode **20**, a bonding pad **42** for the polysilicon gate electrode **40**.

[0016] Referring to FIG. **2** and FIG. **3**, the extended drain region **50** and the drain diffusion region **53** forms the drain electrode **10**. The isolated P-well **65**, the source diffusion region **55** and the contact diffusion region **57** form the source electrode **20**. The bonding pad **12** is connected to the drain metal contact **15** for the drain electrode **10**. The bonding pad **22** is connected to the source metal contact **25** for the source electrode **20**. The bonding pad **42** is connected to the polysilicon gate electrode **40**. The N-well **30** beneath the P-field **60** and divided P-fields **61** and **62** are connected from the drain electrode **10** to the source electrode **20**. The portion of the N-well **30** in between the divided P-fields **61** and **62** reduces the on-resistance of the channel.

[0017] The P-field **60** and the divided P-fields **61** and **62** located in the extended drain region **50** form a junction-field in the N-well **30**. The N-well **30**, the P-field **60**, and the divided P-fields **61** and **62** deplete the drift region, which build the electrical field in the N-well **30** and help to increase the breakdown voltage. In order to get a high breakdown

voltage the extended drain region **50** must be fully depleted before breakdown occurs. The N-well **30**, P-fields **60**, and divided P-fields **61** and **62** enable the extended drain region **50** to be depleted before breakdown occurs even though the doping density of the drift region is high. This allows the drift region to have higher doping density and accomplish low resistance.

[0018] FIG. **4** shows the electrical field distribution when a 650V voltage is applied to the drain region **52** of the LDMOS transistor **100**. The bold dotted lines respectively indicate the potential voltages of 0V, 100V, 200V, 300V, 400V, 500V, 550V, 600V and 650V.

[0019] Furthermore, the portion of the N-well **30** generated by the second diffusion region **37** provides a low-impedance path for the source region **56**, which restricts the transistor current flow from flowing in between the drain region **52** and the source region **56**.

[0020] The LDMOS transistor **100** of the present invention uses a simple structure to implement high breakdown voltage, low on-resistance and isolated performance. Furthermore, the cost is reduced and the production yield can be greatly raised.

[0021] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.